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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,323	01/05/2001	Masatoshi Akagawa	1081.1102	3680

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STAAS & HALSEY LLP
700 11TH STREET, NW
SUITE 500
WASHINGTON, DC 20001

EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,323	AKAGAWA, MASATOSHI	
	Examiner	Art Unit	
	Khi m D Nguy n	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-6 and 14-17 have been considered but are moot in view of the new ground(s) of rejection.

New Grounds of Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (U.S. Patent No. 6,235,554) in view of Itabashi et al. (U.S. Patent No. 6,300,244).

Akram teaches a semiconductor device comprising (See col. 3, line 64 to col. 5, line 34 and FIGS. 1-4):

plural pairs of conductor layers 26 (col. 4, lines 36-39), each pair of conductor layers having wiring patterns and being contained within an insulating layer (44, 46) (col. 4, lines 33-44 and FIG. 1) wherein:

a semiconductor element 14 is imbedded inside the insulating layer (col. 4, lines 25-32 and FIG. 1);

each semiconductor element is electrically connected to a wiring pattern (22, 24) of a respective pair of conductor layers within the respective insulating layer 46 (col. 4, lines 33-41 and FIG. 1); and

the wiring pattern of each pair of conductor layers is electrically connected, by via holes 16, to a wiring pattern of a conductor layer of a different pair of conductor layers having wiring patterns and contained within another insulating layer (col. 4, line 60 to col. 6, line 7 and FIGS. 1-5).

Akram also discloses in (FIG. 4) wherein two or more semiconductor elements, respectively, are imbedded and mounted inside each of the plurality of insulating layers (col. 5, lines 3-7 and FIG. 4).

Akram fails to expressly disclose electrically connecting the wiring pattern to the semiconductor element by flip chip mounting and via an anisotropically conductive film as recited in present claims 4-6.

Itabashi discloses in figures 1-11 and related text electrically connecting a wiring pattern to a semiconductor element by flip chip mounting and, inherently, by an anisotropically conductive film (figure 10 and col. 17, lines 10-30). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Itabashi with the method of Kim in order to provide excellent anti-shock resistance and connection reliability (col. 3, lines 35-45).

It is held that the selection of the semiconductor element thickness is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species. In re Jones, 162USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA1980)(discovery of optimum value of result effective variable in a known process is obvious).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 14-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Akram et al. (U.S. Patent No. 6,235,554).

Akram teaches a semiconductor device comprising (See col. 3, line 64 to col. 5, line 34 and FIGS. 1-4):

a substrate 50;

a first insulating layer (44, 46) (FIG. 1);

a first conductive layer 26 having wiring patterns and formed within the first insulating layer (lowermost package 10C in FIGS. 1-4);

a second conductive layer (middle package 10B) having wiring patterns and formed over the first insulating layer, one or more of the wiring patterns of the second conductive layer being electrically connected to one or more of the wiring patterns of the first conductive layer through via holes 16 (col. 4, line 60 to col. 5, line 34 and FIGS. 1-4);

at least one semiconductor element 14 imbedded within the first insulating layer such that the at least one semiconductor element is electrically connected to at least one

of the wiring patterns of the first conductive layer and at least one of the wiring patterns of the second conductive layer (col. 5, lines 9-17 and FIG. 4); and

a second insulating layer having at least one semiconductor element 14 imbedded therein, the second insulating layer provided on the first insulating layer and containing therein the second conductive layer, and the at least one semiconductor element of the second insulating layer being electrically connected to one or more of the wiring patterns of the first and second conductive layers (col. 4, line 60 to col. 5, line 34 and FIGS. 1-4).

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-6 and 14-17 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's argument that Akram et al. does not teach or suggest, among other things, a semiconductor device comprising plural pairs of conductor layers, each pair of conductor layers having wiring patterns and contained within an insulating layer; wherein: a semiconductor element is imbedded inside each insulating layer, examiner disagreed, Akram et al. disclose a semiconductor device comprising plural pairs of conductor layers 26 (col. 4, lines 36-39), each pair of conductor layers having wiring patterns and contained within an insulating layer (44,46) (col. 4, lines 33-44) and FIGS. 1-4); wherein: a semiconductor element 14 is imbedded inside each insulating layer (col. 4, lines 25-32 and FIGS. 1-4).

In response to applicant's argument that Akram et al. does not teach or suggest among other things, a first insulating layer; a first conductive layer having wiring patterns

and formed within the first insulating layer...and at least one semiconductor element imbedded within the first insulating layer such that the at least one semiconductor element is electrically connected to at least one of the wiring patterns of the first conductive layer and at least one of the wiring patterns of the second conductive layer, examiner disagreed, Akram et al. disclose a first insulating layer (44, 46); a first conductive layer having wiring patterns and formed within the first insulating layer (lowermost package 10C in FIGS. 1-4)...and at least one semiconductor element 14 imbedded within the first insulating layer such that the at least one semiconductor element is electrically connected to at least one of the wiring patterns of the first conductive layer and at least one of the wiring patterns of the second conductive layer (middle package 10B) (col. 4, line 60 to col. 5, line 34 and FIGS. 1-4).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
May 28, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800